**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A thin film capacitor for reducing power source noise connected to a power source, ~~source for reducing power source noise, characterized in that~~ said capacitor ~~has~~ comprising a dielectric thin film, wherein

said dielectric thin film is comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, ~~and~~

said bismuth layer structured compound is expressed by the formula $(Bi_2O_2)^{2+}$ $(A_{m-1}B_mO_{3m+1})^{2-}$ or $Bi_2A_{m-1}B_mO_{3m+3}$, where the symbol m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, ~~and W.~~ and W,

said dielectric thin film further includes at least one rare earth element Re selected from Sc, Y, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu, and

an amount of substitution by the rare earth element Re, X, is in the range of (i) $0.4 \leqq X \leqq 1.8$ in the formula $Bi_2A_{2-x}Re_xB_3O_{12}$ when the symbol m is equal to 3, and (ii) $0.01 \leqq X \leqq 2.0$ in the formula $Bi_2A_{3-x}Re_xB_4O_{15}$ when the symbol m is equal to 4.

2. (Original) The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor is a decoupling capacitor connected in parallel between the power source and an integrated circuit.

3. (Withdrawn) The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor is a bypass capacitor connected in parallel between the power source and an integrated circuit.

4. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is arranged near an integrated circuit chip.

5. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is arranged in contact with an integrated circuit chip.

6. (Withdrawn) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is arranged between an integrated circuit chip and a circuit board.

7. (Withdrawn) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is mounted buried in a recess of a circuit board.

8. (Withdrawn) The thin film capacitor for reducing power source noise as set forth in any one of claim 2, wherein said capacitor is mounted on the surface of a circuit board.

9. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is formed integrally inside a circuit board.

10. (Withdrawn) The thin film capacitor for reducing power source noise as set forth in claim 2, wherein said capacitor is arranged at an inside or surface of a connection socket.

11. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor has a lower electrode formed on said thin film forming substrate, said dielectric thin film formed on said lower electrode, and an upper electrode formed on said dielectric thin film.

12. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor has a multilayer structure comprised of a plurality of said dielectric films stacked via electrodes.

13. (Previously Presented) The thin film capacitor for reducing power source noise as set forth in claim 1, wherein said capacitor is comprised of a bismuth layer structured compound having a c axis orientation of at least 80%.